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'**Peer Reviewed Journal IJERA com**
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Volume 1 Device Interfaces and
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May 11th, 2018 - arithmetic core lphaAdditional info FPGA provenWishBone Compliant NoLicense LGPLDescriptionRTL Verilog code to perform Two Dimensional Fast Hartley Transform 2D FHT for 8x8 points Presented algorithm is FHT with decimation in frequency domain Main FeaturesHigh Clock SpeedLow Latency 97 clock cycles Low Slice CountSingle Clock Cycle per'

'**Software Patent Eligibility at the Federal Circuit 2017**
December 17th, 2017 - If there was a theme that emerged in software patent eligibility cases during 2017 it was the need to have what is innovative disclosed in the claims'

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